REMARKS

Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks. Applicant thanks the Examiner for withdrawing the previous objections to the title, drawings and specification. Applicant also thanks the Examiner for withdrawing the previous rejections under 35 USC 101 and 112.

Claims 1, 12 and 15 have been amended. Claims 1, 5-12 and 14-18 remain pending.

Claims 1-11 stand objected to due to typographical errors in claim 1. The Examiner has requested a correction and Applicant has amended claim 1 to correct the typographical errors. Applicant respectfully requests the objection to claim 1 be withdrawn and that claims 1-11 be reconsidered.

Claim 15-18 stands rejected under 35 U.S.C. 112, first paragraph. Applicant requests claims 15-18, as amended, be reconsidered as set forth in more detail below.

Claims 1-18 stand rejected under 35 U.S.C. 102(b). Applicant traverses this rejection as set forth in more detail below.

Amendments

Revisions to the Specification and Drawings

The Examiner requested correction of certain errors in the specification and drawings. In response, Applicant has amended the specification and drawings accordingly. No new matter has been added. The amendments are supported in the drawings or elsewhere in the specification.

Amendments to the Claims

Applicant has amended the claims to more particularly point out what Applicant regards as the invention. No new matter has been added as a result of these amendments.

Rejections

Rejections under 35 U.S.C. §112, First Paragraph

Claims 15-18 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner is unclear as to the

evidence for "logic" as stated in claim 15. Applicant has amended claim 15 to more particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically the term logic was replaced with the phrase "computer readable code stored on a computer readable medium." The phrase "computer readable code stored on a computer readable medium" is supported in paragraph 38. Accordingly, Applicant requests this rejection be withdrawn and amended claims 15-18 be reconsidered.

Rejections under 35 U.S.C. §102(b)

Claims 1-18 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Hennessy et al (Computer Architecture: A quantitative Approach). Applicant respectfully traverses the rejection in view of the amended claims 1, 5, 6, 10-12, 14 and 15.

The Hennessey reference outlines the basic functionality of a pipeline processing, specifically that the instructions are staged in pipeline stages for execution.

The Applicant's invention is a system and method for implementing swap requests to provide a constant latency of two clock cycles and an ability to launch a swap request every clock cycle. Each swap request includes 2 different instructions: a save instruction and a restore instruction.

A swap request ***is not the same*** as the "MOVI2S" and "MOVS2I" instructions described by Hennessy and relied on by the Examiner.

A save instruction moves the contents of the active register to a selected one of 8, or possibly 4, window registers. A restore instruction moves the contents of a different window register to the active register.

The save instruction and the restore instruction for the corresponding swap request ***occur in 2 consecutive clock cycles***. As a result, each swap request must require two clock cycles. A swap request is broken into save and restore instructions that happen in consecutive clock cycles in the address decode implementation for swap requests.

Therefore, a constant swap request latency of 2 clock cycles is achieved by internal pipelining of swap instructions and throughput every clock cycle to launch a new swap instruction. For example, the restore instruction for first swap request

(SWAP A), and the save instruction for second swap request (SWAP B) occur simultaneously. See Figure 2A of the Applicant's application and the related description.

Applicant respectfully submits that the examiner is interpreting Hennessy excessively broadly. The move instructions, "MOVI2S" and "MOVS2I," described by Hennessey and relied on by the examiner are not the same as the swap requests described by the Applicant. The move instruction merely moves the contents of one register to another register.

In stark contrast, each and every swap request includes a precise sequence of a *save instruction* ***immediately followed*** *by a restore instruction.* Therefore, to execute multiple swap requests in successive clock cycles requires that the restore instruction of the first swap request be executed at the same time as the save instruction of the second swap request.

Further, when the restore instruction for first swap request (SWAP A) and the save instruction for second swap request (SWAP B) occur simultaneously, they can be executed in a single hardware register or latch.

Nothing in the Hennessey reference teaches or even suggests four instructions being executed in this manner to complete two successive swap requests.

As to claims 1, 12 and 15, the Hennessy reference does not teach nor even suggest a pipeline architecture or a method for processing a plurality of swap requests including receiving a first swap request in a pipeline wherein the first swap request requests swapping active contents of an active register window with a first contents from a first register and executing the first swap request. Executing the first swap request includes executing a first save operation wherein the active contents of the active register window is saved to corresponding register and executing a first restore operation, wherein the first contents of the first register are restored to the active register window. The method also includes receiving a second swap request in the pipeline immediately subsequent to the first swap request, wherein the second swap request requests swapping the first contents in the active register window with a second contents from a second register. The first register is examined to determine if the first register is a same register as the second register. The second swap request is executed if the first swap request and the second swap request do not swap the same register. Executing the second swap request includes executing a second save

operation wherein the first contents of the active register window is saved to the first register substantially simultaneously with the executing the first restore operation and executing a second restore operation, wherein the second contents of the second register are restored to the active register window.

The Hennessey reference does not teach nor even suggest each and every limitation as recited in claims 1, 12 and 15.

Accordingly, Applicant respectfully submits that Applicant's invention as claimed in claims 1, 12 and 15 and those claims that depend from one of claims 1, 12 and 15 are patentable over the Hennessey reference, and respectfully request the withdrawal of the rejection under 35 U.S.C. §102(b).

SUMMARY

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact George B. Leavell at (408) 749-6900, ext 6923.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 50-0805 (Ref # SUNMP351) for any charges that may be due or credit our account for any overpayment. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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